REMARKS

Claims 2-3 and 13-14 have been canceled. Thus, claims 1, 4-12, and 15-16 are pending in the present application. In the Office Action, claims 1, 11, and 12 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Kodaira, et al (U.S. Patent No. 4,835,734). Claims 2-10 and 13-16 were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Kodaira in view of Christenson, et al (U.S. Patent No. 6,574,721). Claims 2-3 and 13-14 have been canceled, rendering the Examiner's rejections of these claims moot. The Examiner's remaining rejections are respectfully traversed.

With regard to independent claims 1, 11, and 12, Applicants describe and claim receiving a virtual address, comparing at least a portion of the virtual address to a first preselected range, and using a paging mechanism to generate a first physical address from the virtual address in response to the virtual address being outside the first preselected range. Applicants also describe and claim using a hard mapped mechanism to generate a second physical address from the virtual address in response to the virtual address being within the first preselected range. As defined at lines 3-7 on page 9 of the Patent Application, "hard mapping" comprises locating the physical addresses (which are stored in a locked page translation mechanism by a secure kernel) corresponding to the virtual addresses falling within a preselected range at a particular location in physical memory that does not vary during the operation of the data processor (i.e., no swapping occurs).

Kodaira is directed to a virtual memory space that is divided into two ranges 30, 31. Kodaira teaches that a logical address 80 is divided into portions 81, 82. When the portion 81 is all zeros, a first segment table 11 is used to translate the logical address into an address corresponding to the range 31. When the portion 81 is not all zeros, a second segment table 12 is

used to translate the logical address into an address corresponding to the range 30. See, Kodaira, Figures 1 and 2 and related discussion. However, as admitted by the Examiner, Kodaira fails to teach using a paging mechanism or a hard mapped mechanism to generate a physical address. For at least the aforementioned reasons, Applicants respectfully submit that claims 1, 11, and 12 are not anticipated by Kodaira and request that the Examiner's rejections of these claims be withdrawn.

Moreover, it is respectfully submitted that the pending claims are not obvious in view of the cited references, either alone or in combination. To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). There must also be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. That is, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986).

As discussed above, Kodaira fails to teach using a paging mechanism or a hard mapped mechanism to generate a physical address. The Examiner therefore relies upon Christenson to teach using a paging mechanism or a hard mapped mechanism to generate a physical address. Christenson is directed to providing simultaneous local and global addressing capabilities in a computer system. Christenson notes that virtual addressing schemes map virtual address spaces onto physical (real) address spaces. See Christenson, col. 1, ll. 49-59. However, contrary to the Examiner's allegation, Christenson does not teach or suggest a hard mapping mechanism, as defined in the Patent Application. Moreover, Christenson fails to teach or suggest using a hard

mapped mechanism to generate a second physical address from the virtual address in response to the virtual address being within the first preselected range. Thus, Applicants respectfully submit that the cited references fail to teach or suggest all the claim limitations.

Christenson also teaches translating a virtual address to a physical address using a page table if the virtual address is not out of range, i.e. if the virtual address does not span beyond a segment (subdivision) boundary defined within the global addresses. However, if the virtual address is out of range, an interrupt is generated to indicate an addressing error. A page fault routine may also be called to try to load a page into memory. See Christenson, col. 10, ll. 51-63. Thus, Christenson appears to teach away from the claimed invention by teaching that an interrupt is generated in response to determining that the virtual address is out of range. In particular, Christenson appears to teach away from using a paging mechanism to generate a first physical address from the virtual address in response to the virtual address being outside the first preselected range. It is by now well established that teaching away by the prior art constitutes *prima facie* evidence that the claimed invention is not obvious. *See, inter alia, In re Fine*, 5 U.S.P.Q.2d (BNA) 1596, 1599 (Fed. Cir. 1988); *In re Nielson*, 2 U.S.P.Q.2d (BNA) 1525, 1528 (Fed. Cir. 1987); *In re Hedges*, 228 U.S.P.Q. (BNA) 685, 687 (Fed. Cir. 1986).

For at least this reason, Applicants respectfully submit that claims 1, 11, 12, and all claims depending therefrom are not obvious over Kodaira in view of Christenson and request that the Examiner's rejection of claims 4-10 and 15-16 under 35 U.S.C. § 103(a) be withdrawn.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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